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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/872,924	06/01/2001	James J. deBlanc	10007686-1	3268

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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	5

DATE MAILED: 12/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,924	DEBLANC ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

On page 6, Table 2 : State / LOW; Current / 0μA < Lih < -1 mA; it does not make sense in light of the Current value range.

On page 10, line 12, substitute "VTH 520 and RTH 530" by --VTH 530 and RTH 520--.

Appropriate correction is required.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description:

The reference sign 220 and 230 in Fig. 2 are not used in the text disclosure.

A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to under 37 CFR 1.83(a) because they fail to show the isolation circuitry comprising active components as described in the specification (See Application page 11, lines 25-27 and Claim 10). Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 4, 7 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "approximately" in claim 4, 7 and 15 is a relative term which renders the claim indefinite. The term "approximately" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. In this case, the claims 4 and 15 recite the subject matter "a value in a range of approximately 1 KΩ to 25 KΩ", and the claim 7 recites the subject matter "a value in a range of approximately 10 Ω to 5 KΩ". However, the term "approximately" in the claims makes the claims indefinite, respectively, because no one could define the values of "approximately 10 Ω" and "approximately 1 KΩ".

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1-4, 8, 9, 12-15, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al. [US 6,603,323 B1; hereinafter Miller] in view of Bittner, Jr. [US 6,434,647 B1; hereinafter Bittner].

Referring to claims 1 and 12, Miller discloses a backplane apparatus (i.e., interconnect system 66 of Fig. 7) comprising: a common bus (i.e., a set of buses 91-94 in Fig. 7) comprising a plurality of signal lines (i.e., bus 91, 92, 93 and 94 in Fig. 7); and isolation circuitry (i.e., isolation resistor 78 in Fig. 7) for electrically coupling each of said plurality of signal lines of said common bus to a corresponding plurality of signal lines (See Fig. 7) of an electronic device (i.e., integrated circuit 62 in Fig. 7) to enable communication between said common bus and said electronic device through said isolation circuitry (See col. 6, lines 42-52).

Miller does not expressly teach each signal line of said common bus having a current limiting element, RA, which is a first current limiting element.

Bittner discloses a reflected-wave bus termination (See Abstract), wherein a termination circuit 130 (Fig. 1) having a current limiting element, RA (i.e., resistor 132 of Fig. 1) coupled to each signal line (i.e., individual signal line 14 in Fig. 1) of a common bus (i.e., digital communication bus 10 of Fig. 1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said termination circuit, as disclosed by Bittner, in said common bus, as disclosed by Miller, for the advantage of allowing reflected waves to be utilized for reflected-wave switching, while preventing continued ring-ing which might otherwise disrupt proper switching on said common bus (See Bittner, col. 2, lines 65-67).

Referring to claims 2 and 13, Miller teaches a plurality of connectors (i.e., pads 80 in Fig. 7) for removably coupling said plurality of signal lines of said electronic device to said plurality of signal lines of said common bus through said isolation circuitry (See Fig. 7 and col. 6, lines 45-52).

Referring to claim 3, Miller teaches said isolation circuitry for each signal line comprises an inline resistor, RD (i.e., isolation resistors 78 in Fig. 7).

Referring to claim 8 and 19, Miller teaches isolation circuitry (i.e., isolation resistor 78 in Fig. 7) for at least one signal line has no pull up resistor (i.e., no pull up registers are coupled to said common bus; See interconnect structure 66 in Fig. 7).

Referring to claim 9, Miller teaches said isolation circuitry (i.e., isolation resistor 78 in Fig. 7) comprises passive components (i.e., resistors).

Referring to claim 14, Miller teaches said isolation circuitry (i.e., isolation resistor 78 in Fig. 7) coupling said corresponding signal lines comprises an inline resistor, RD, for each signal line (i.e., isolation resistors 78 in Fig. 7).

Referring to claims 4 and 15, Miller teaches RD has a value of 1 KΩ (See col. 3, lines 33-39; i.e., a value in a range of approximately 1 KΩ to 25 KΩ).

Referring to claim 18, Bittner teaches RA (i.e., resistor 132 of Fig. 1) for each selected signal line of said common bus is selected to have a value of 47 Ω (See col. 4, lines 28-31; i.e., a value in a range of approximately 10 Ω to 5 KΩ).

9. Claim 5-7, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller [US 6,603,323 B1] in view of Bittner [US 6,434,647 B1] as applied to claims 1-4, 8, 9, 12-15, 18 and 19 above, and further in view of Garlepp et al. [US 2001/0035768 A1; hereinafter Garlepp].

Referring to claims 5 and 16, Miller, as modified by Bittner, discloses all the limitations of the claims 5 and 16, respectively, except that does not expressly teach isolation circuitry for at least one of said signal lines further comprises a pull up resistor.

Garlepp discloses an output driver circuit (See Abstract), wherein an isolation circuitry (i.e., series resistor R_s and parallel resistor R_p in clock driver circuit 71 of Fig. 5) comprising a pull up resistor (i.e., parallel resistor R_p in Fig. 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said pull-up resistor, as disclosed by Garlepp, in said isolation circuitry for at least one of said signal lines, as disclosed by Miller, as modified by Bittner, so as to closely match the loaded impedance of at least one of said signal lines, which reduces signal jitter (i.e., clock jitter) by minimizing the occurrence of secondary reflections on said signal line (i.e., clock line; See Garlepp, Paragraph [0039]).

Referring to claim 6, Miller teaches said isolation circuitry comprises an inline resistor, RD (i.e., isolation resistors 78 in Fig. 7).

Referring to claim 7, Bittner teaches RA (i.e., resistor 132 of Fig. 1) has a value of 47 Ω (See col. 4, lines 28-31; i.e., a value in a range of approximately 10 Ω to 5 KΩ).

Referring to claim 17, Miller, as modified by Bittner, discloses all the limitations of the claim 17 except that does not said RD has a value less than 1 KΩ. However, the claim recites said value less than 1 KΩ without any patentable advantage in the specification (See claim 17 and Application page 10, lines 26-27). Therefore, the limitation of said value less than 1 KΩ in the claim is not patentably significant since it at most relates to the typical value of depending on circuit design under consideration which is not ordinarily a matter of invention. *In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141.*

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller [US 6,603,323 B1] in view of Bittner [US 6,434,647 B1] as applied to claims 1-4, 8, 9, 12-15, 18 and 19 above, and further in view of Wiggers [US 6,011,710 A].

Referring to claim 10, Miller, as modified by Bittner, discloses all the limitations of the claim 10 except that does not expressly teach said isolation circuitry comprising active components.
Wiggers discloses a capacitance reducing memory system (See Abstract), wherein an isolation circuitry (i.e., switches 29 in Fig. 4; See col. 5, lines 14-19) comprising active components (i.e., FET type switches; See col. 4, lines 53-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said passive type isolation circuitry (i.e., isolation resistor 78 in Fig. 7), as disclosed by Miller, by said active type isolation circuitry (i.e., FET type switches 29 in Fig. 4), as disclosed by Wiggers, for the advantage of allowing said backplane apparatus (i.e., memory system) configuration to be easily changed by simply adding said electronic devices (i.e., modules) or by replacing some or all of said electronic devices (See Wiggers, col. 4, lines 61-65).

11. Claims 11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller [US 6,603,323 B1] in view of Bittner [US 6,434,647 B1] as applied to claims 1-4, 8, 9, 12-15, 18 and 19 above, and further in view of what was well known in the art, as exemplified by Fisher et al. [US 5,572,685 A; hereinafter Fisher].

Referring to claims 11 and 20, Miller, as modified by Bittner, discloses all the limitations of the claims 11 and 20, respectively, except that does not expressly teach said electronic device is a disk drive. The Examiner takes Official Notice that said electronic device being a disk drive, is well known to one of ordinary skill in the art, as evidenced by Fisher (See Fig. 1 and col. 3, lines 15-32).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have included said disk drive in said backplane apparatus as said electronics device since it would provide a large capacity of non-volatile memory array.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

With regard to Bus Termination,

Feldbaumer [US 5,382,841 A] discloses switchable active bus termination circuit.

Novak [US 5,721,497 A] discloses cold termination for a bus.

Bonnella et al. [US 6,369,605 B1] disclose self-terminated driver to prevent signal reflections of transmission between electronic devices.

With regard to Bus Speed-Up Circuit,

Inoue [US 6,140,850 A] discloses serial bus speed-up circuit.

Millar [US 5,945,886 A] discloses high-speed bus structure for printed circuit boards.

Kamiya [US 6,531,901 B2] discloses high-speed bus capable of effectively suppressing a noise on a bus line.

With regard to Passive Component Device Network,

Takada et al. [US 5,224,021 A] discloses surface-mount network device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
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cel/ CEL

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